

WHAT IS CLAIMED IS:

1. A delay time estimation method for
estimating a delay time in a logic circuit that
5 includes a MOS transistor, comprising the steps of:
modeling the MOS transistor by a
resistive element having fixed resistance and a
power source voltage that varies with time; and
segmenting an operating characteristic
10 of the MOS transistor thus modeled into a first
region in which a current increases as a gate
potential varies, a second region corresponding to
a saturation region of the MOS transistor in which
region the current gradually decreases as the gate
15 potential remains constant, and a third region
corresponding to a linearity region of the MOS
transistor in which region the current decreases as
the gate potential remains constant.

20 2. The delay time estimation method
according to claim 1 adapted for a circuit in which
a plurality of logic circuits that includes MOS
transistors, comprising the steps of:

segmenting an operating characteristic
25 of last-stage MOS transistor constituting a logic
circuit of a last stage into a first region in
which a current increases as a gate potential
varies, a second region corresponding to a
saturation region of the last-stage MOS transistor
30 in which region the current gradually decreases as

a gate potential remains constant and a third region corresponding to a linearity region of the last-stage MOS transistor in which region the current decreases as the gate potential remains
 5 constant.

3. The delay time estimation method according to claim 1, wherein

10 $E = R_s \times i(t) + v(t)$

holds for $t = \Delta t_1$ and $t = \Delta t_1 + \Delta t_2$, where E denotes the power source voltage, R_s denotes resistance of a model of the power source, $i(t)$ denotes a charge
 15 current of a load model, $v(t)$ denotes a charge voltage of the load model, and wherein

V_1 , Δt_1 and Δt_2 are determined based on a fact that values of $E - v(t)$ and $i(t)$ reside on an $I_{ds} - V_{ds}$ characteristic curve at a given gate
 20 potential, where I_{ds} denotes a drain-source current and V_{ds} denotes a drain-source voltage, and where

V_1 denotes a voltage at a boundary between the first region and the second region, Δt_1 denotes a time required to arrive at the boundary,
 25 and Δt_2 denotes time required to reach the power source voltage via the second region.

4. The delay time estimation method according to claim 1 which employs a delay library
 30 including function information for specifying

polygonal lines that provide a model of an I_{ds} - V_{ds} characteristic at a given potential and also including function information related to a slew rate specifying a fixed delay.

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5. A recording medium storing a computer program that allows a computer to perform the delay time computation method according to claim 1.